FIG. 1

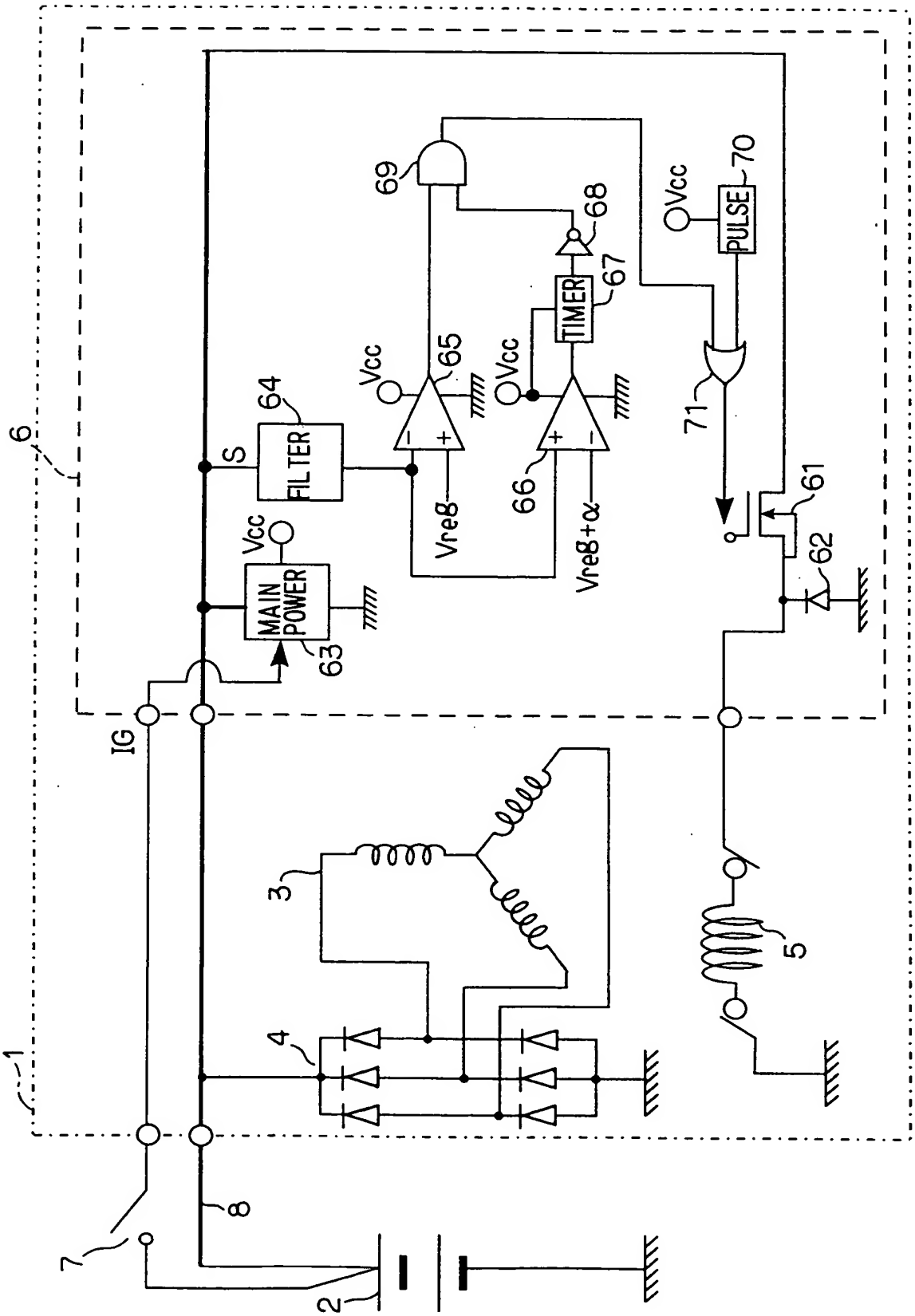

1
2
3
4
5
6
7
8
IG
S
FILTER
64
MAIN POWER
63
Vcc
65
Vcc
66
Vcc
TIMER
67
68
69
PULSE
70
71
61
62
Vref
Vref+α

FIG. 2

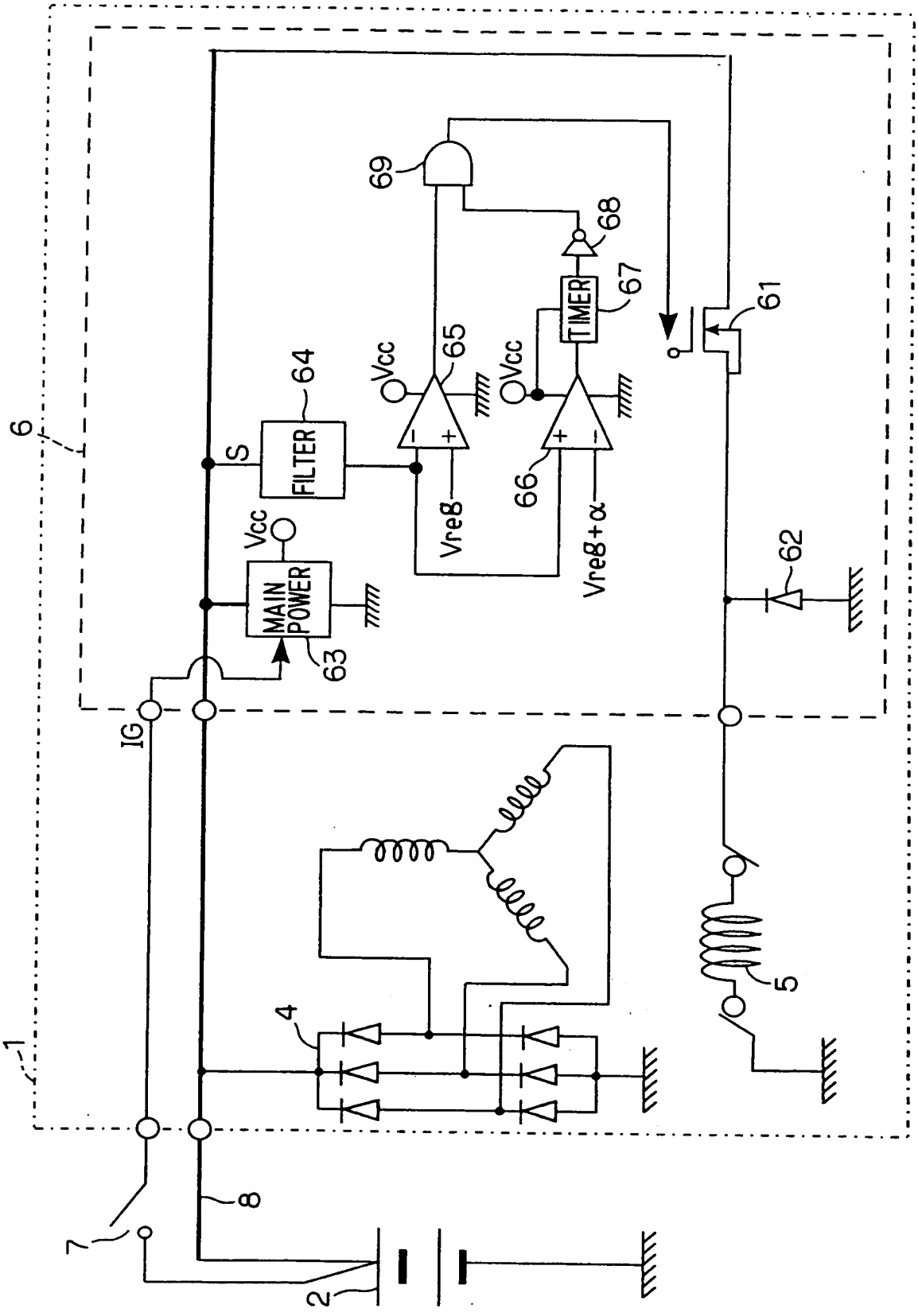

1
2
4
5
6
7
8
IG
S
FILTER
64
Vcc
65
Vcc
66
TIMER
67
68
69
61
62
MAIN POWER
63
Vreg
Vreg+α

FIG. 3

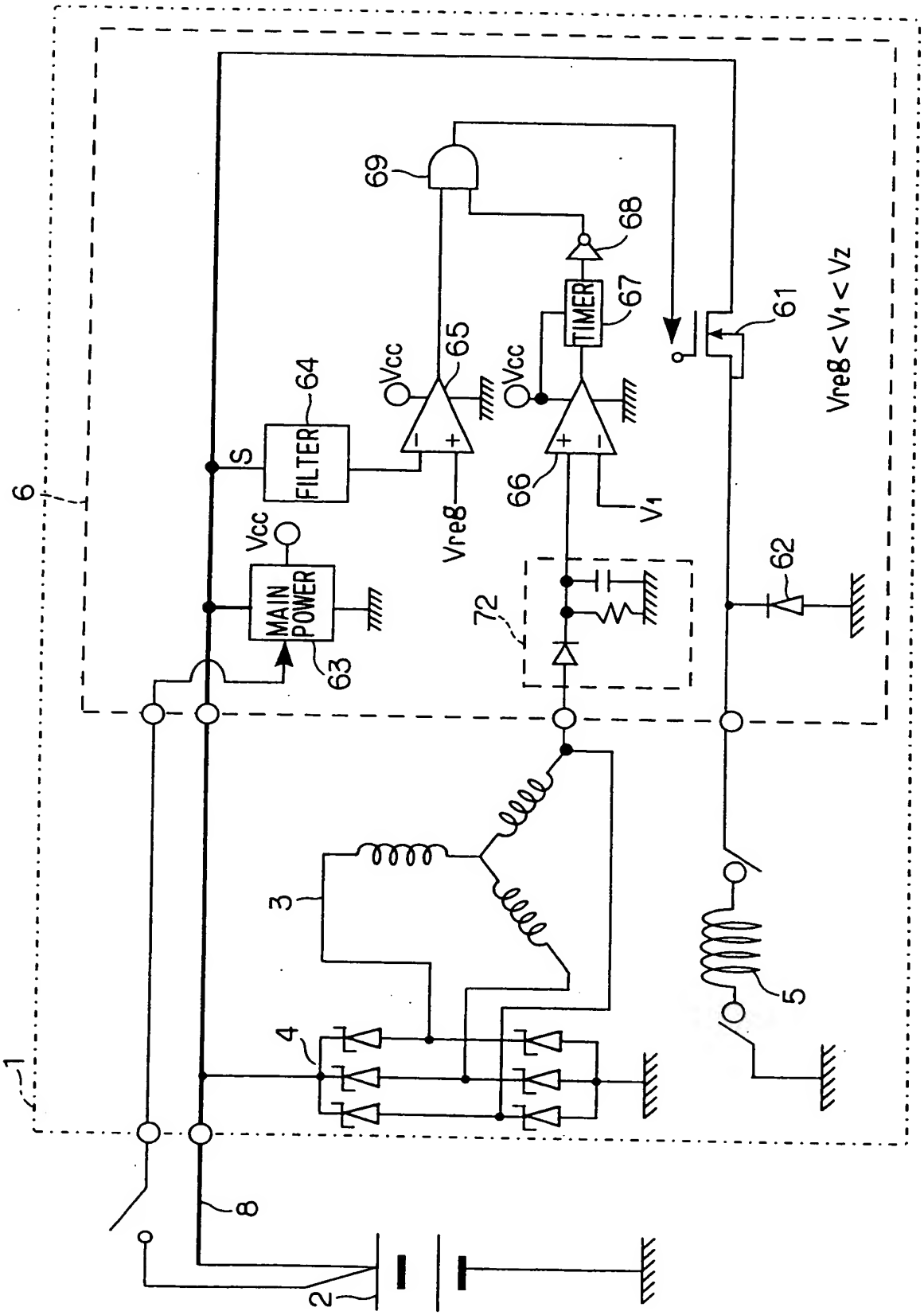

6
1
2
8
3
4
5
61
62
63
64
65
66
67
68
69
72
S
FILTER
MAIN POWER
TIMER
Vcc
Vcc
Vcc
Vref
V1
Vref < V1 < Vz

FIG. 4

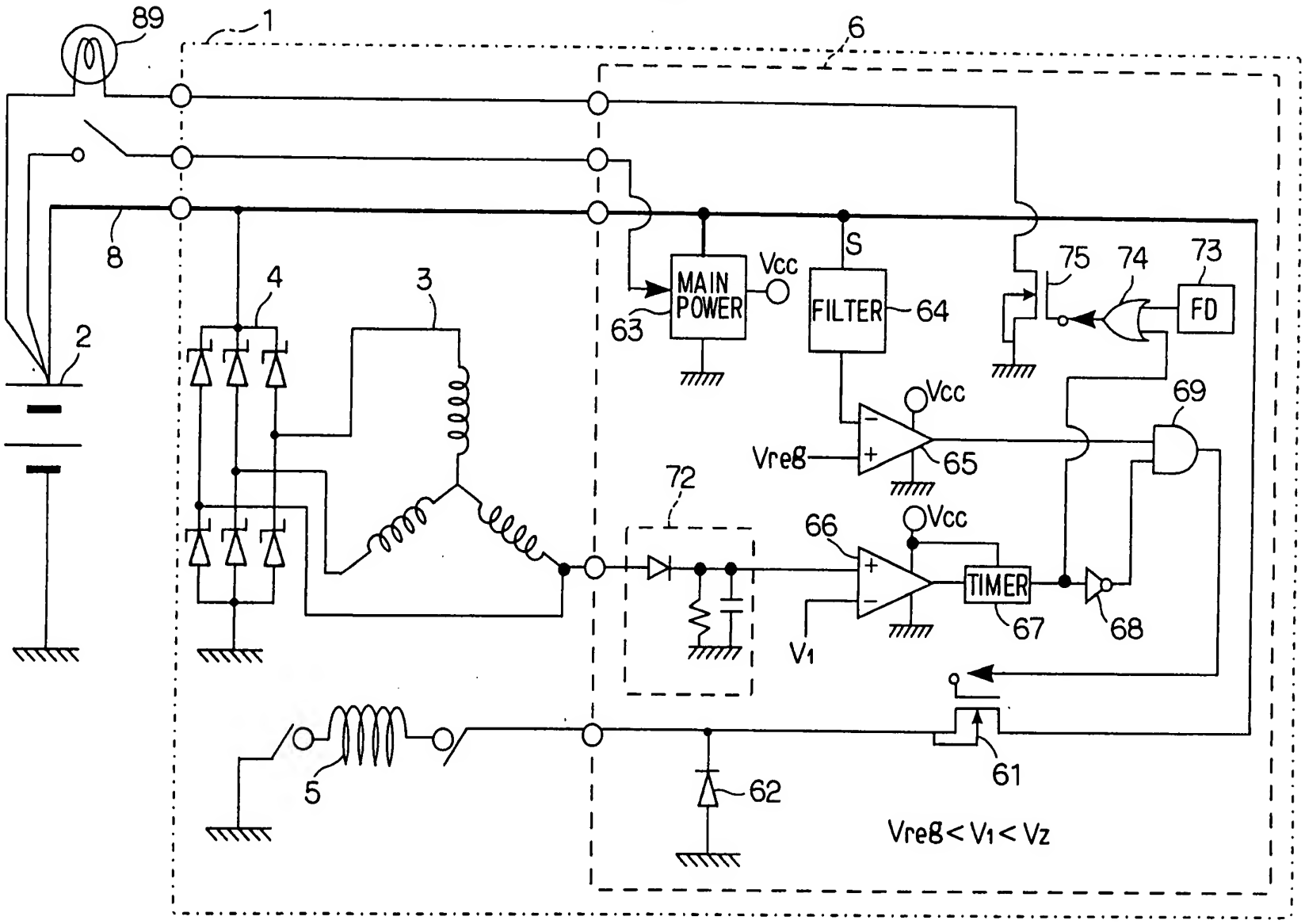

89
1
6
8
4
3
2
MAIN POWER
Vcc
63
S
FILTER
64
75
74
73
FD
Vcc
69
Vreg
65
72
66
Vcc
TIMER
67
68
V1
5
62
61
Vreg < V1 < Vz

FIG. 5

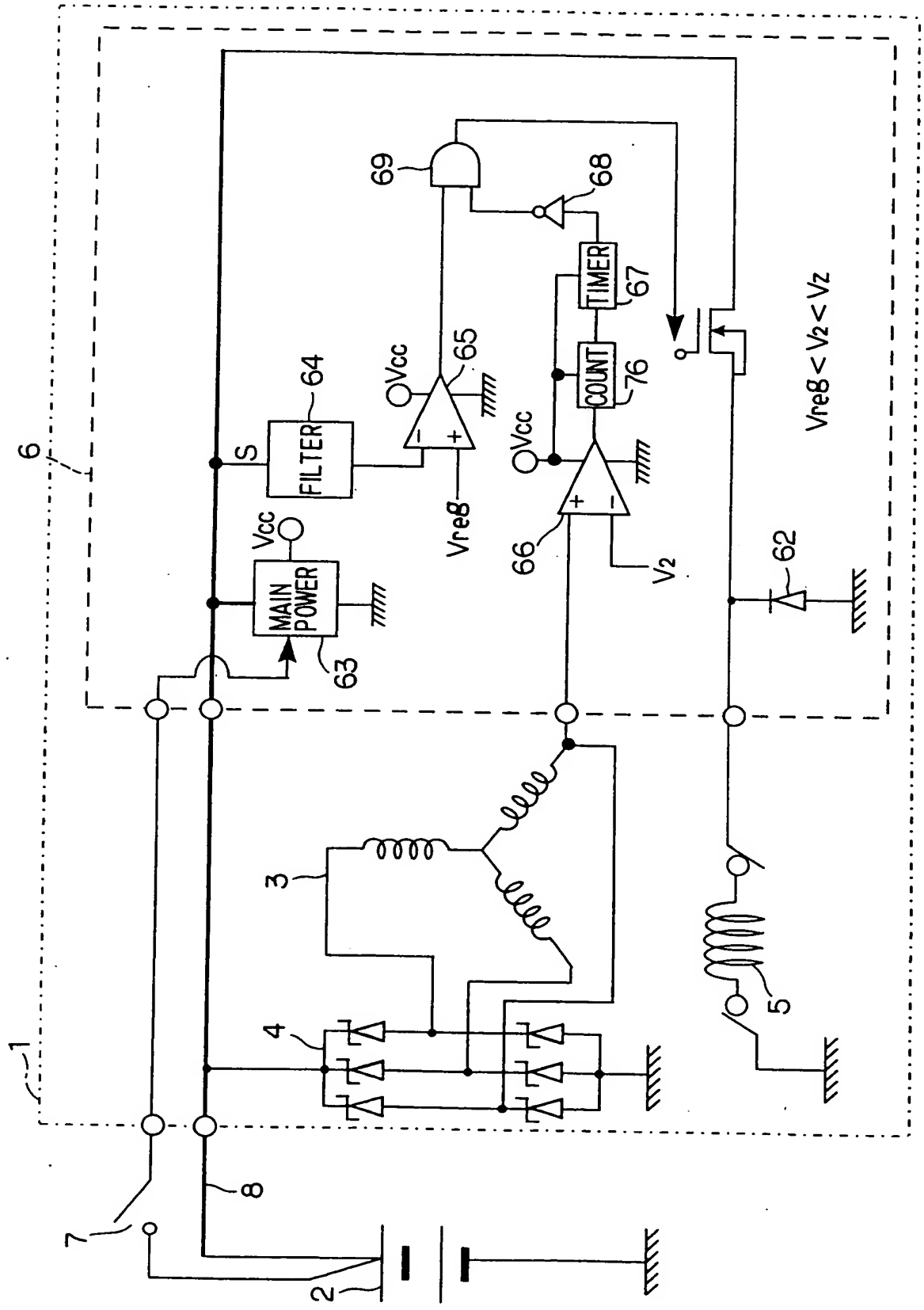

1
2
3
4
5
6
7
8
62
63
64
65
66
67
68
69
76
FILTER
MAIN POWER
TIMER
COUNT
Vcc
Vre8
V2
S
Vre8 < V2 < Vz

FIG. 6

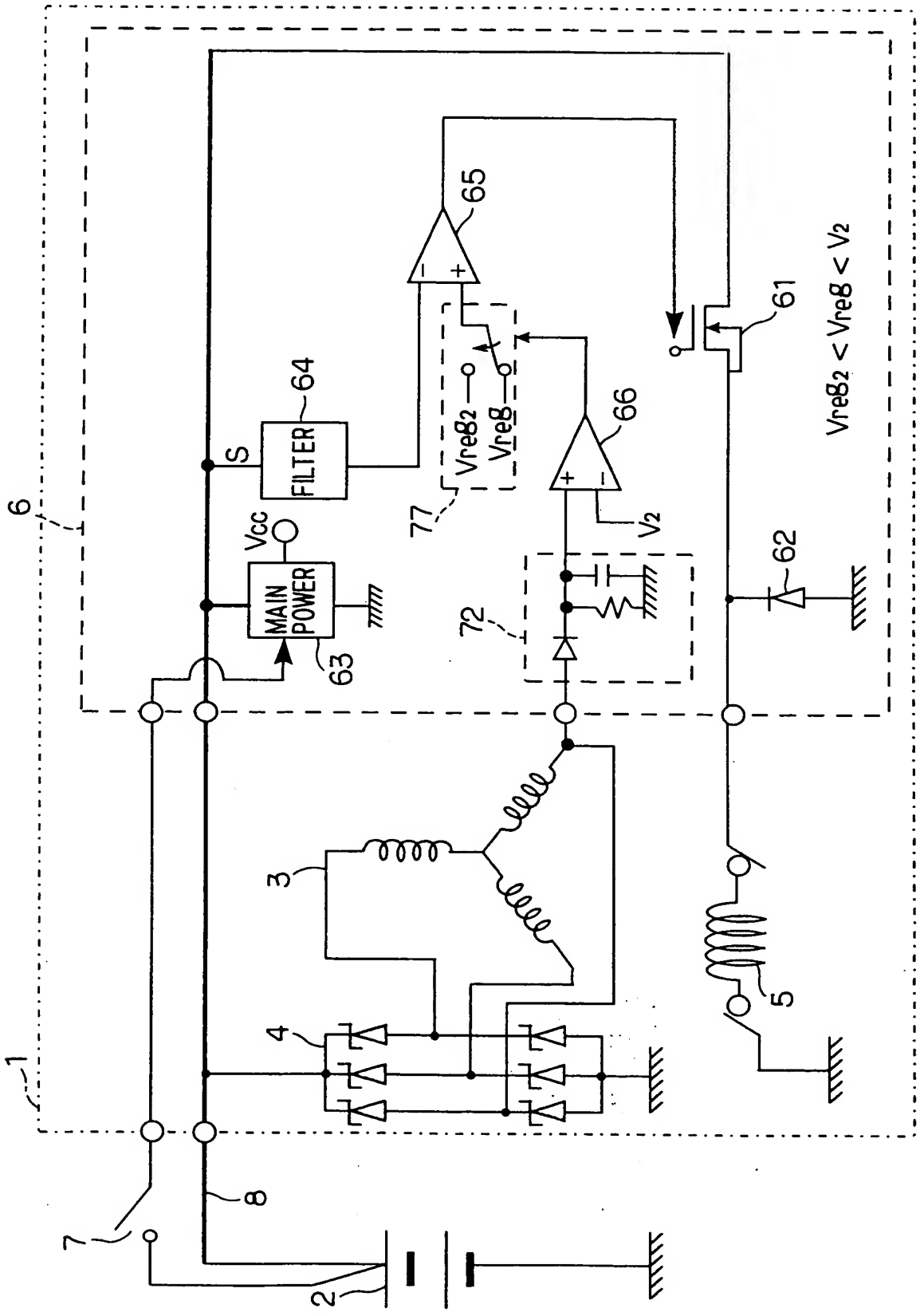

6
1
65
64
FILTER
S
Vcc
MAIN POWER
63
77
Vref2
Vref
66
V2
61
Vref2 < Vref < V2
62
72
3
4
5
7
8
2

FIG. 7

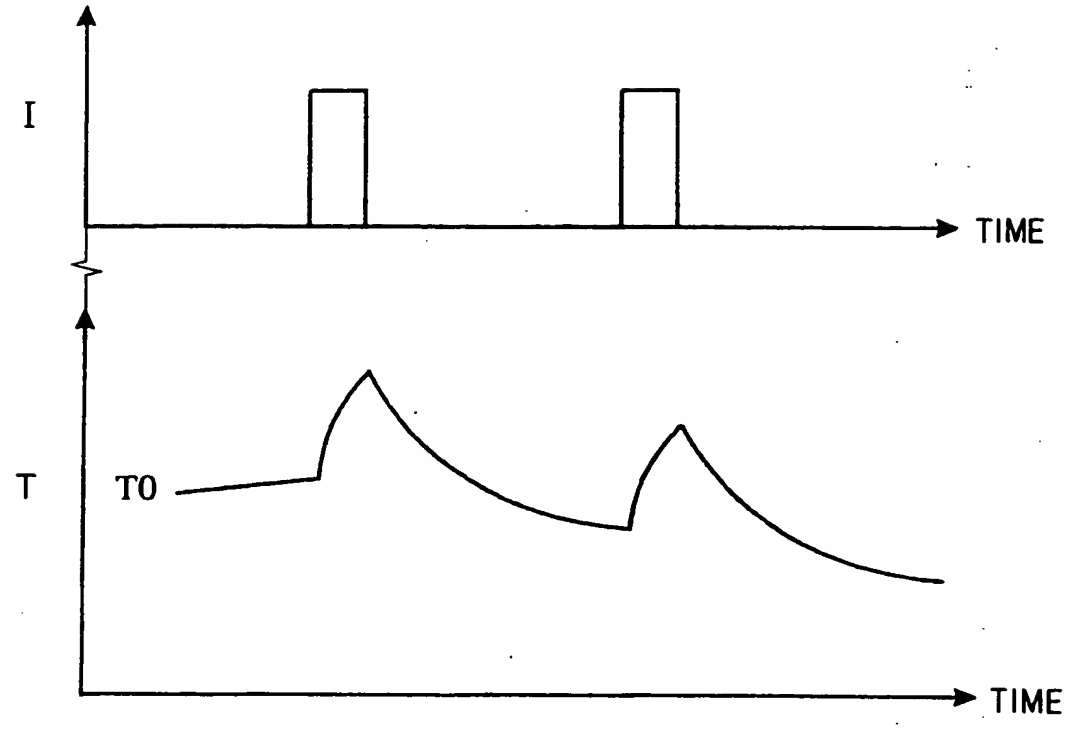


FIG. 22 PRIOR ART

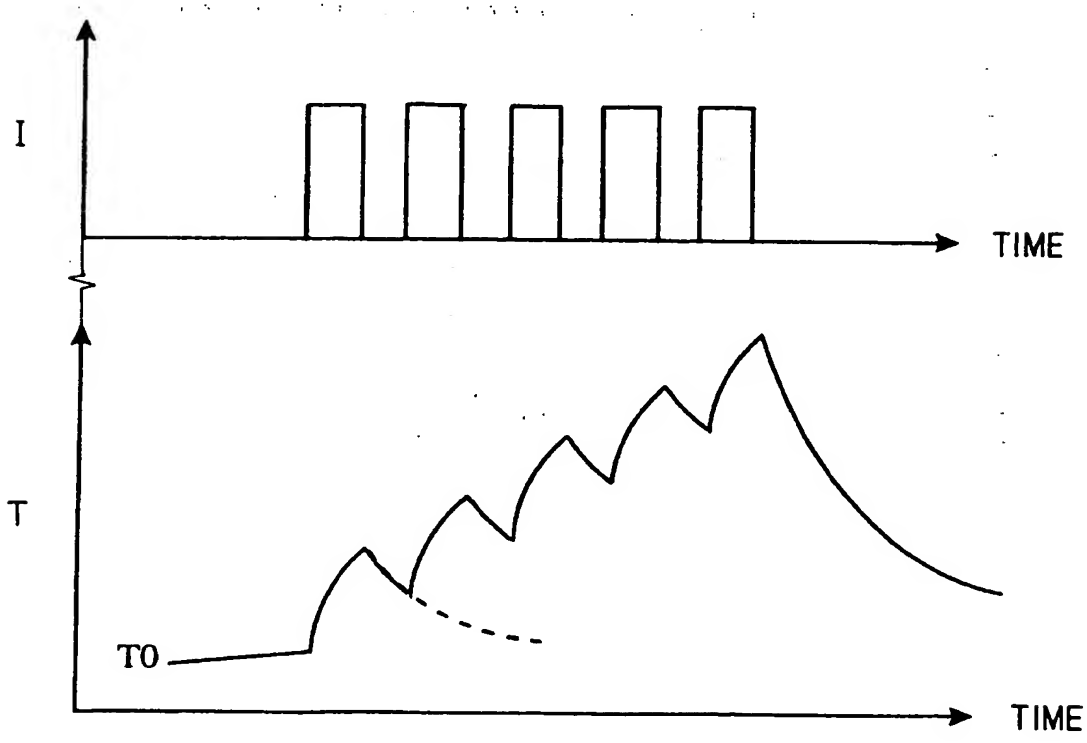


FIG. 8

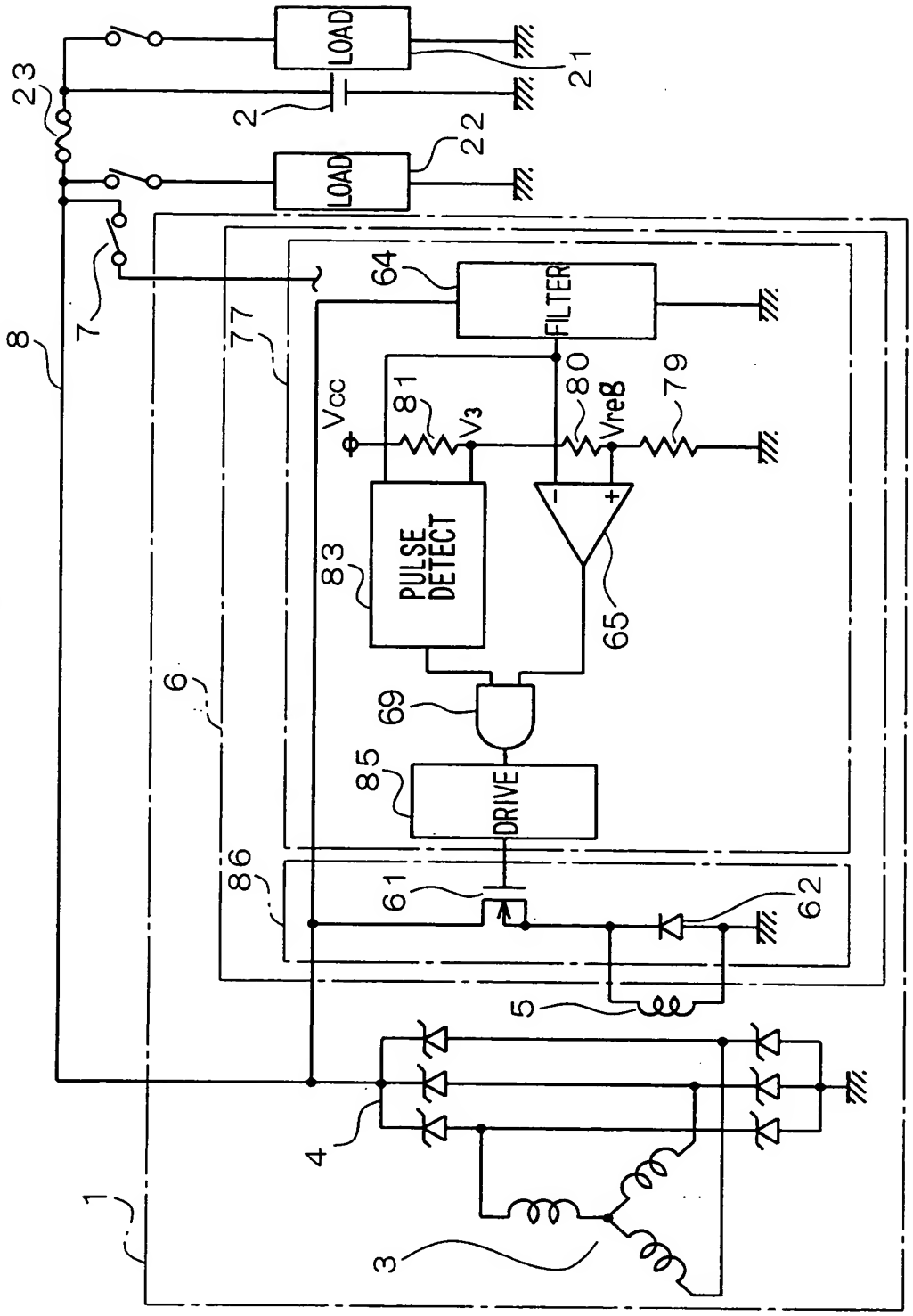

LOAD
LOAD
FILTER
PULSE DETECT
DRIVE
Vcc
V3
Vref
1
2
3
4
5
6
7
8
21
22
23
61
62
64
65
69
77
79
80
81
83
85
86

FIG. 9

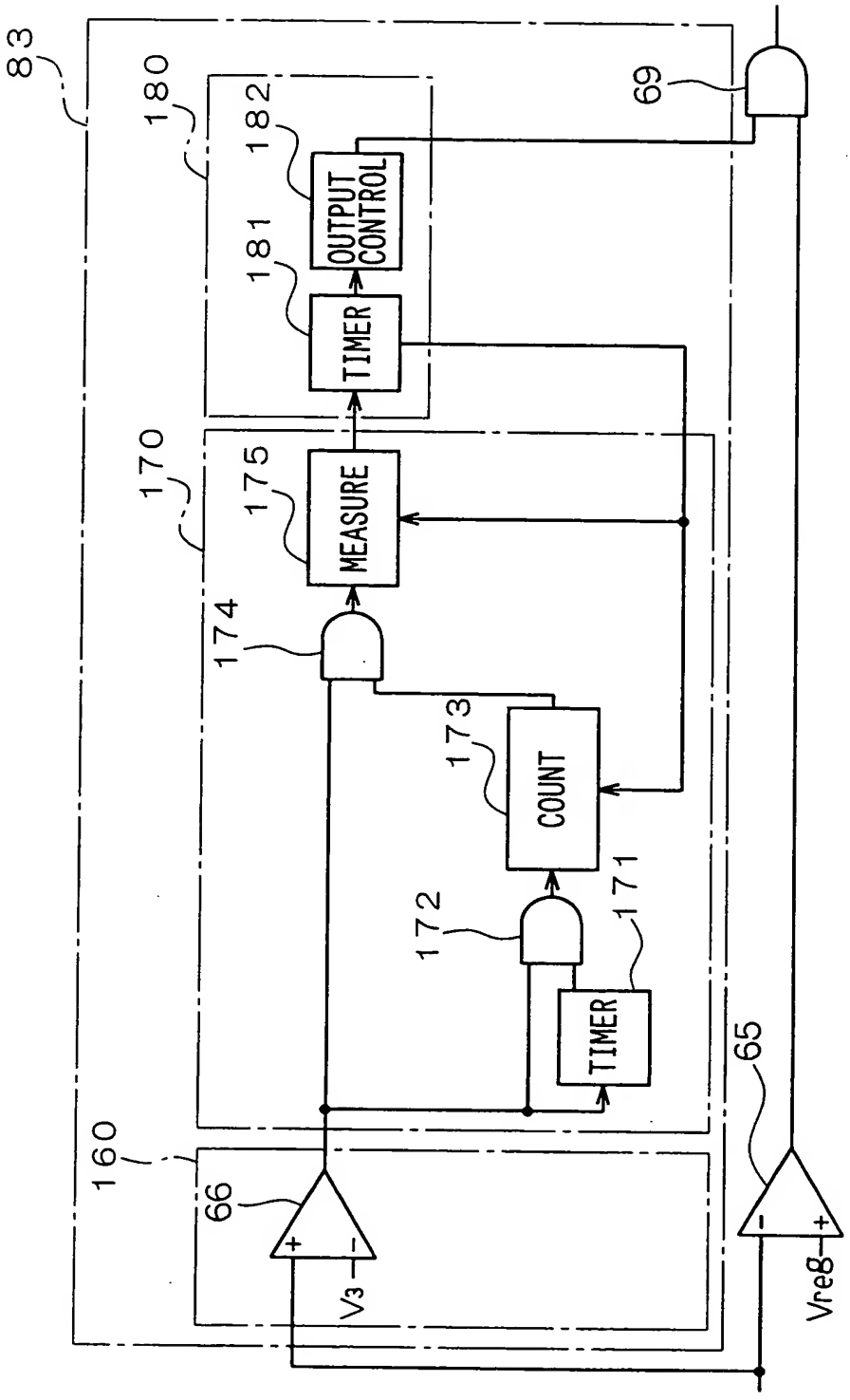

83
180
182
OUTPUT CONTROL
181
TIMER
69
170
175
MEASURE
174
173
COUNT
172
171
TIMER
160
66
65
V3
Vref

FIG. 10

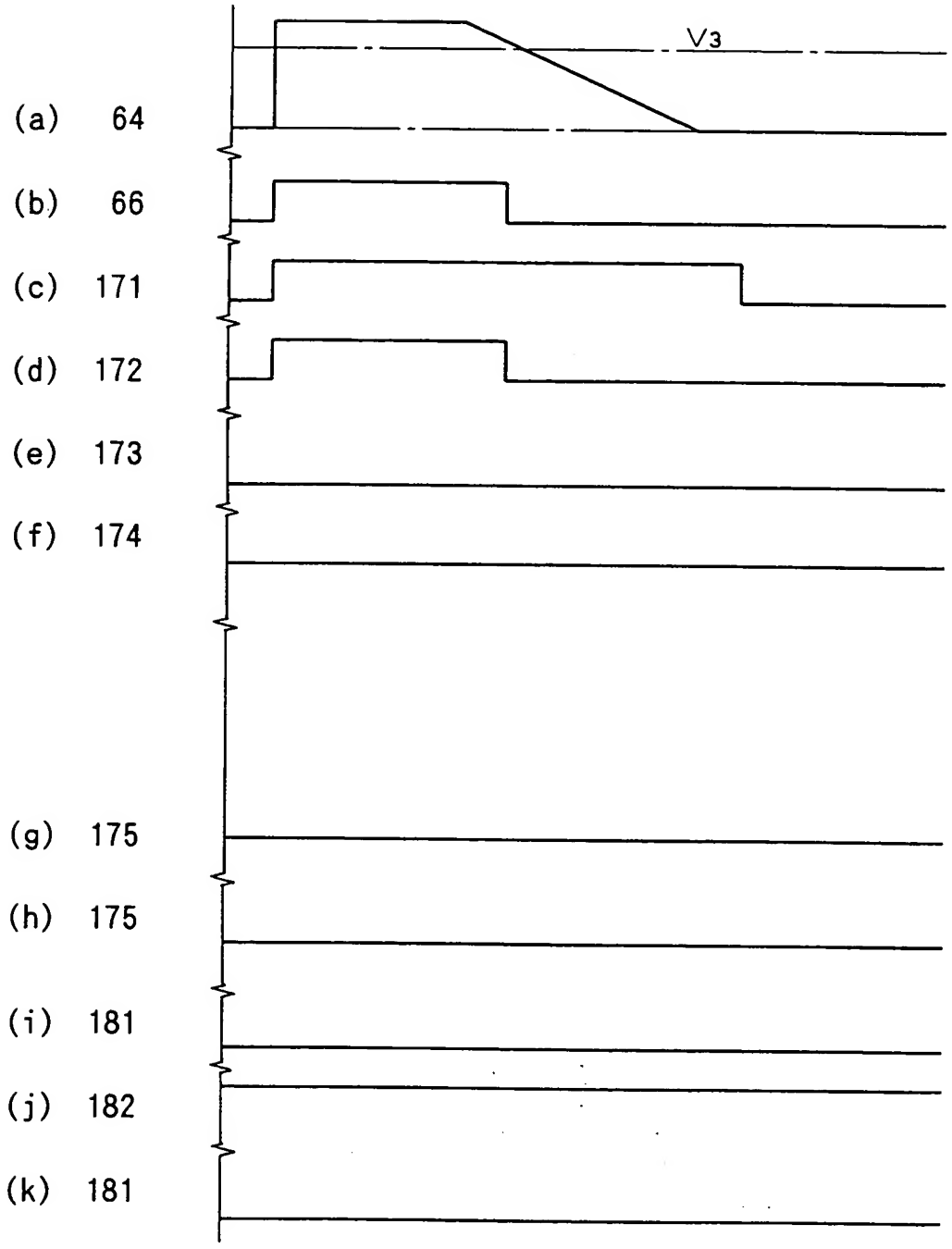


FIG. 11

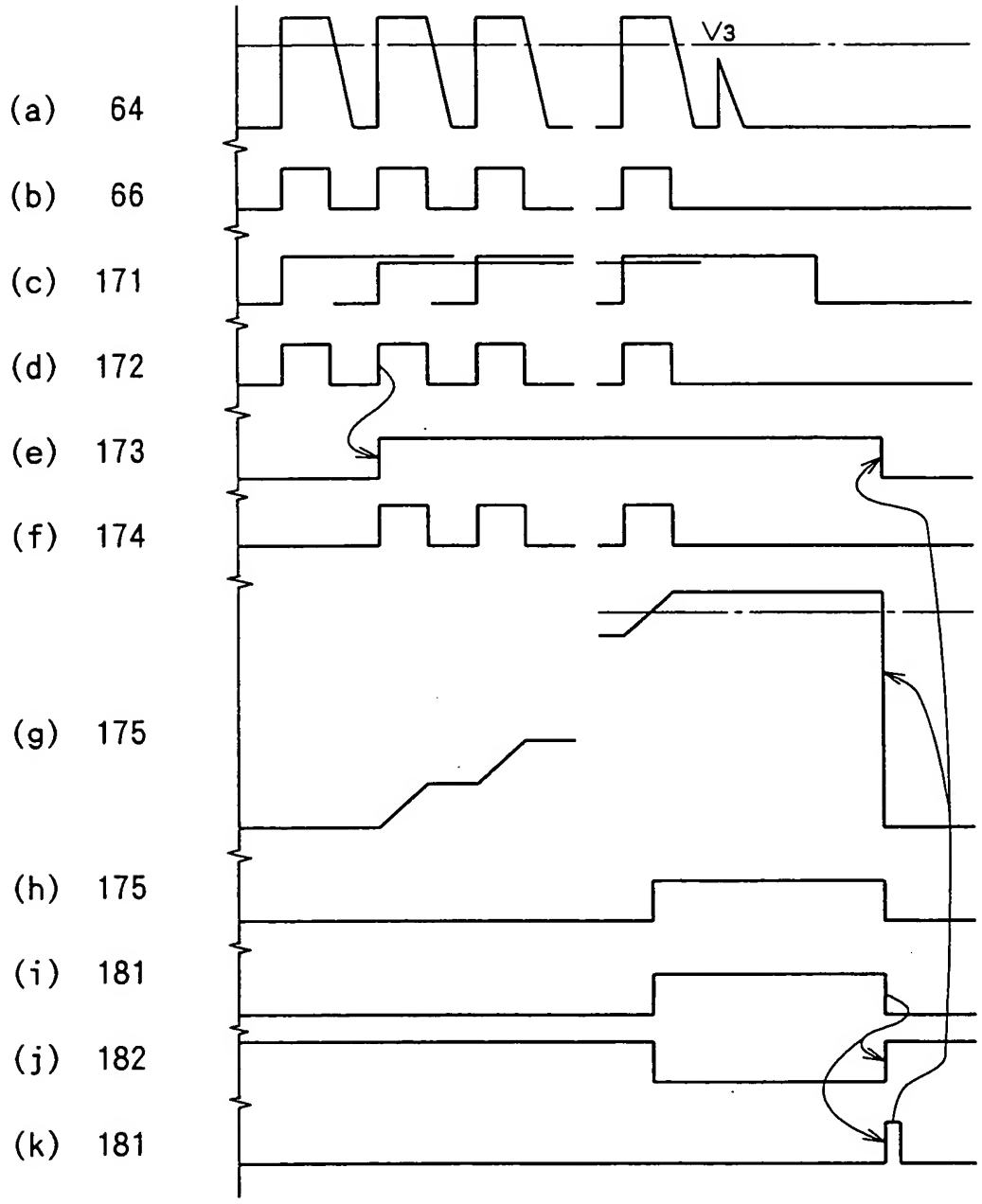


FIG. 12

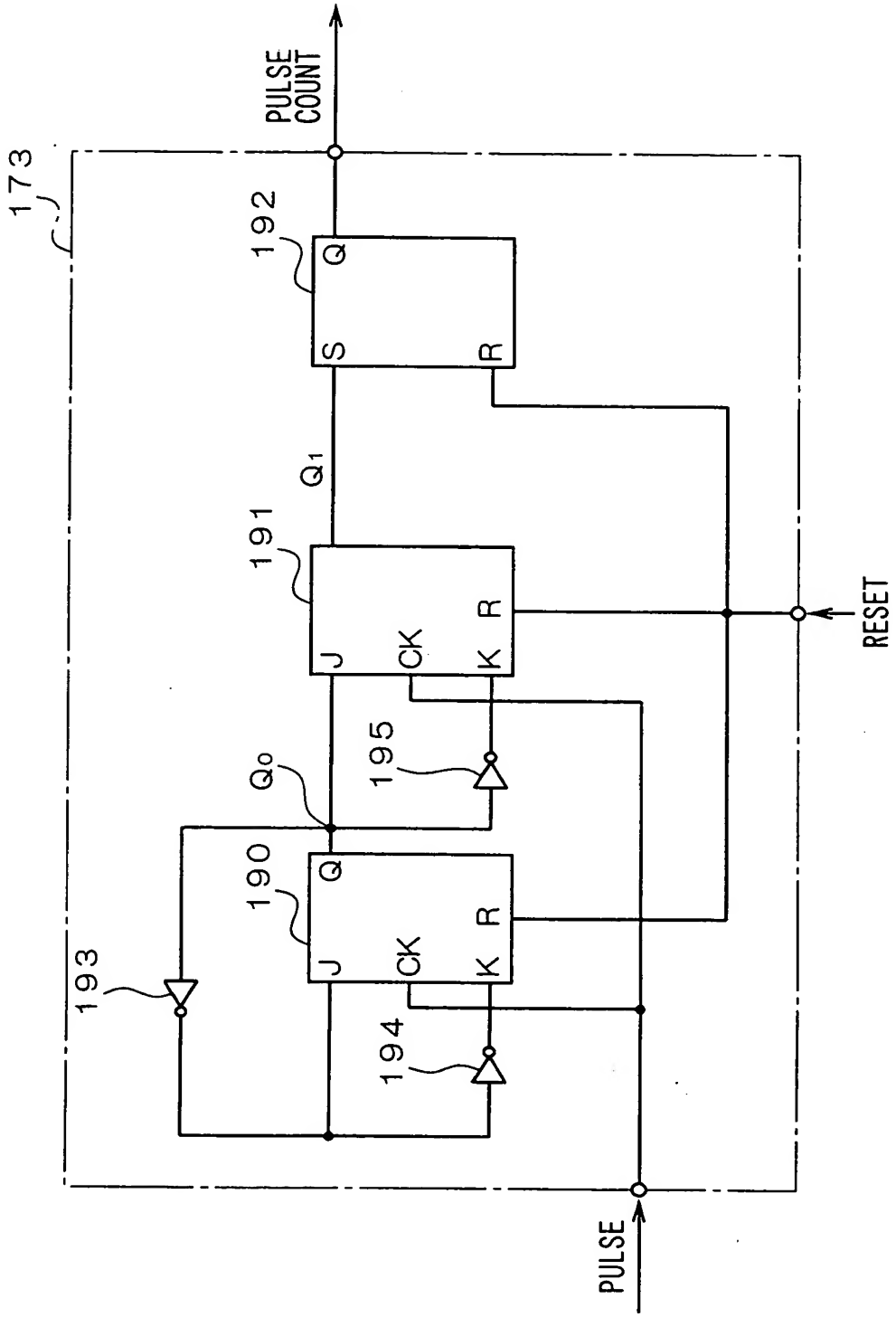

PULSE COUNT
173
192
Q
S
R
Q1
191
J
CK
K
R
RESET
195
Q0
190
Q
J
CK
K
R
193
194
PULSE

FIG. 13

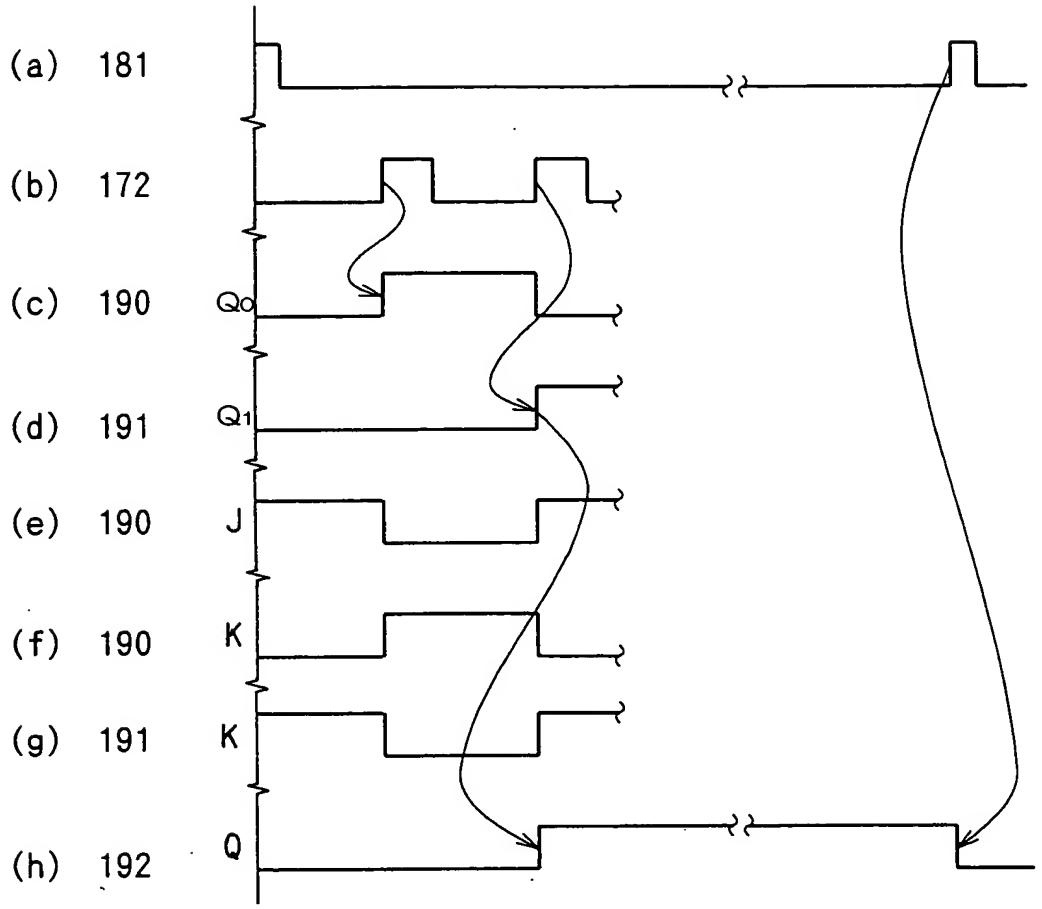


FIG. 14

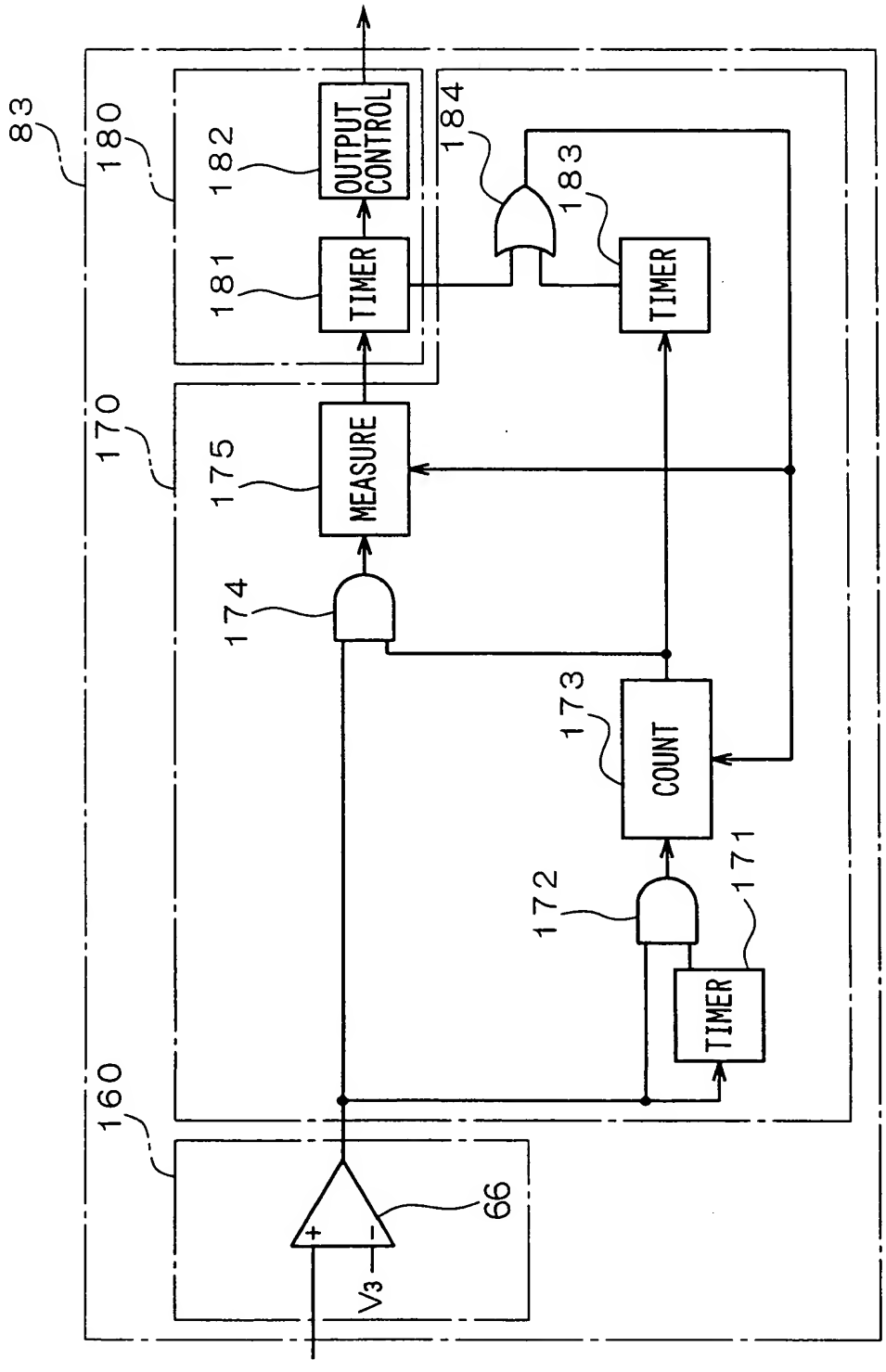

83
180
182
OUTPUT CONTROL
184
183
181
TIMER
TIMER
170
175
MEASURE
174
173
COUNT
172
171
TIMER
160
66
+
-
V3

FIG. 15

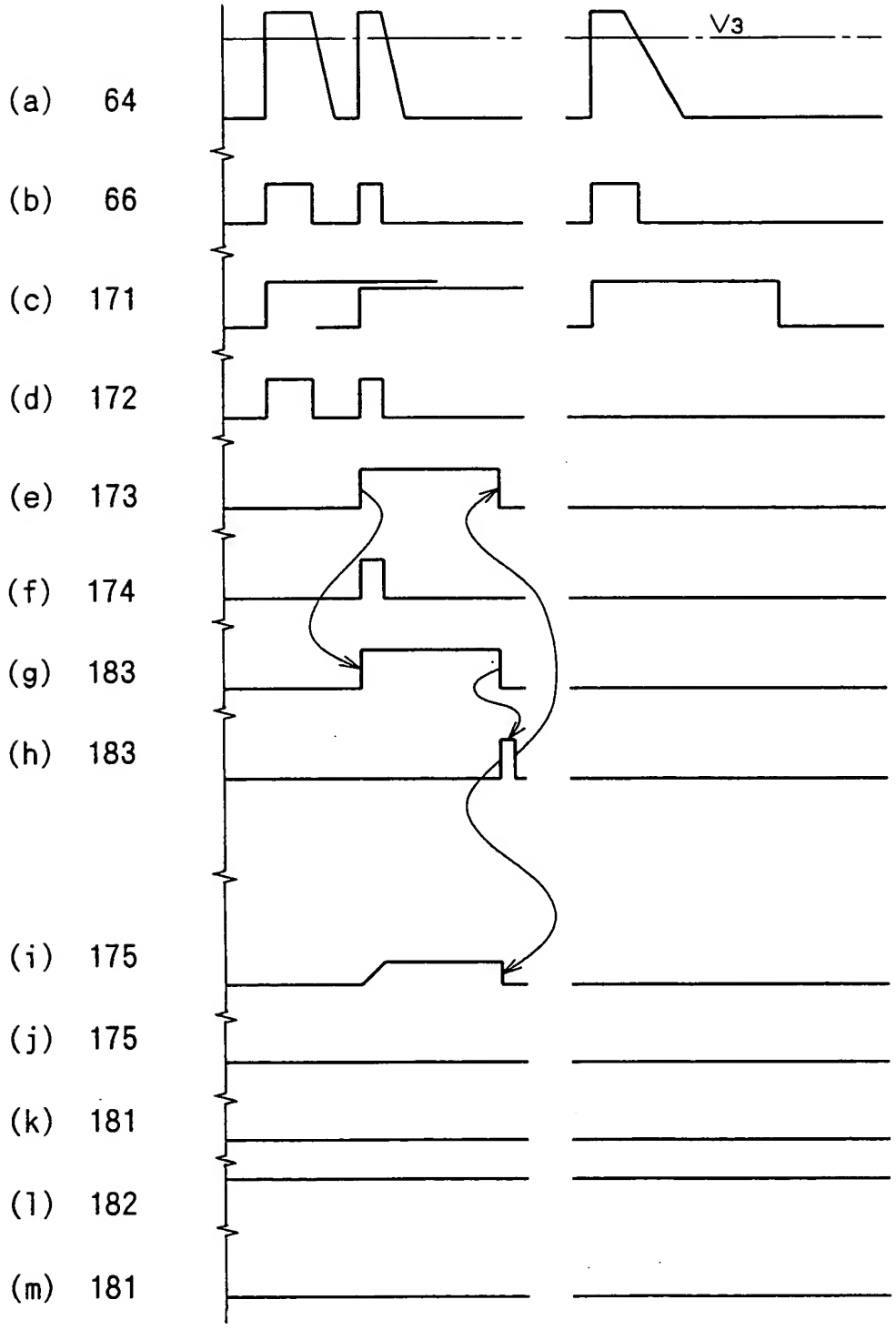

V3
(a) 64
(b) 66
(c) 171
(d) 172
(e) 173
(f) 174
(g) 183
(h) 183
(i) 175
(j) 175
(k) 181
(l) 182
(m) 181

FIG. 16

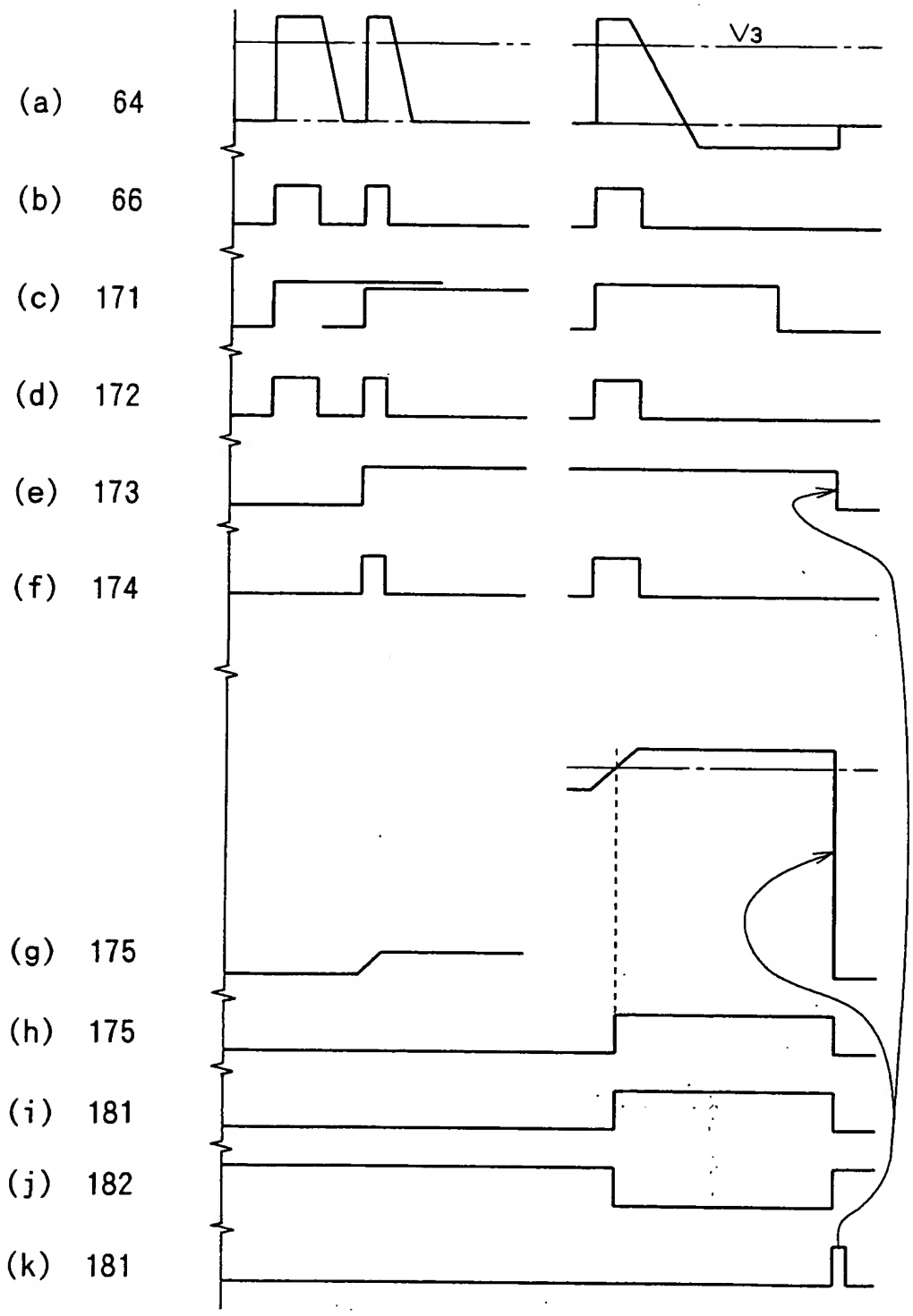


FIG. 17

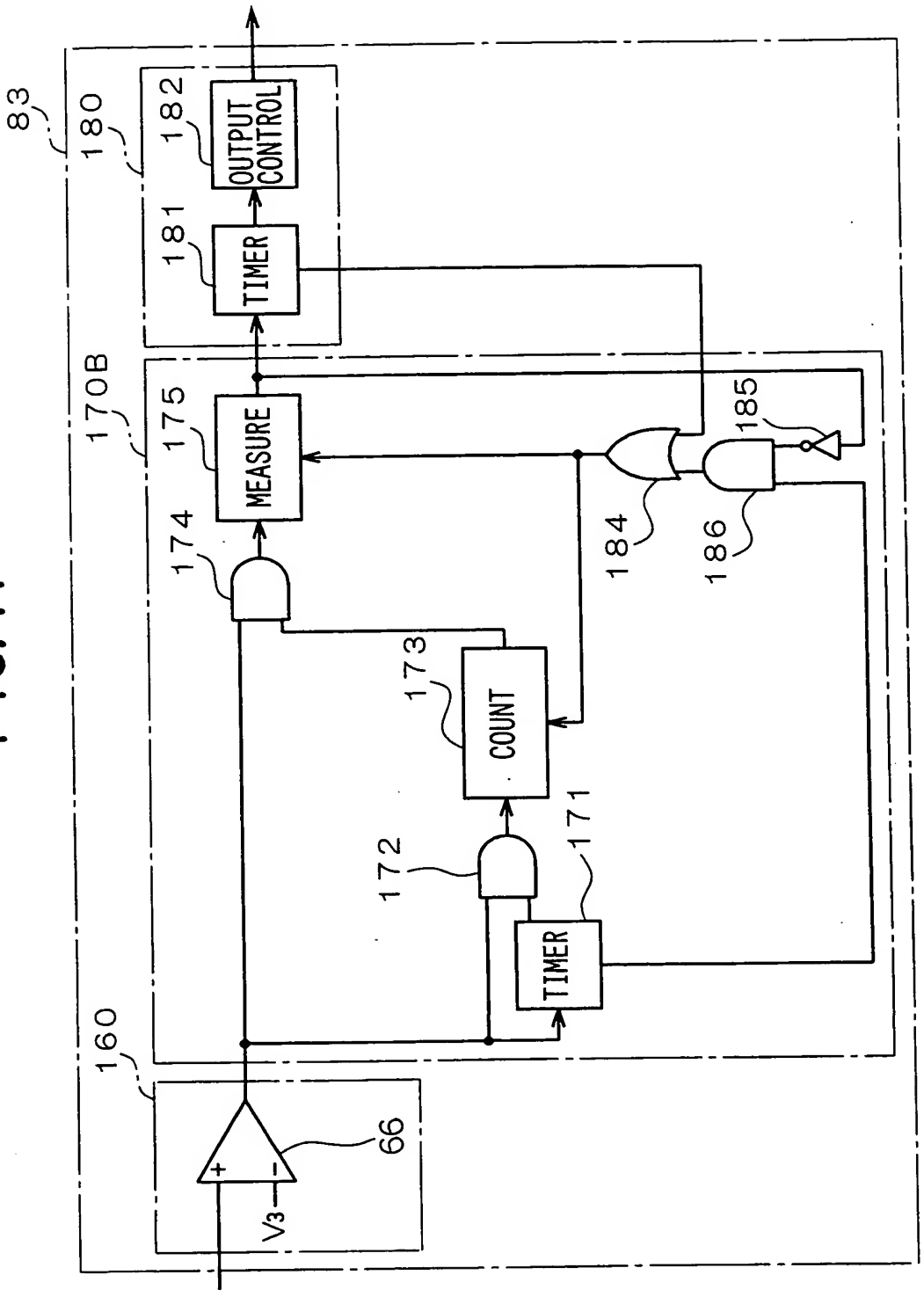

83
180
182
OUTPUT CONTROL
181
TIMER
170B
175
MEASURE
185
174
184
186
173
COUNT
172
171
TIMER
160
66
+
-
V3

FIG. 18

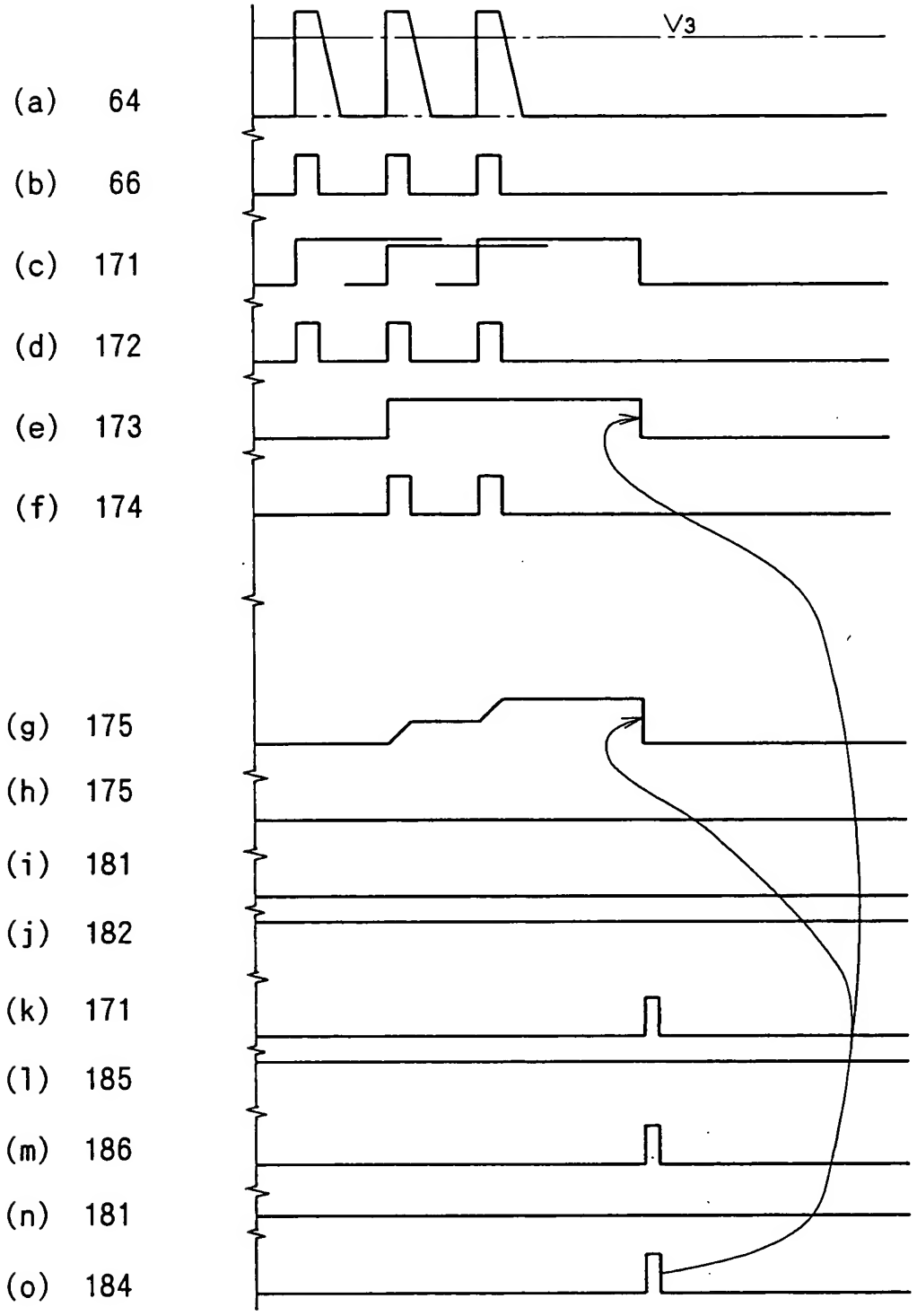

V3
(a) 64
(b) 66
(c) 171
(d) 172
(e) 173
(f) 174
(g) 175
(h) 175
(i) 181
(j) 182
(k) 171
(l) 185
(m) 186
(n) 181
(o) 184

FIG. 19

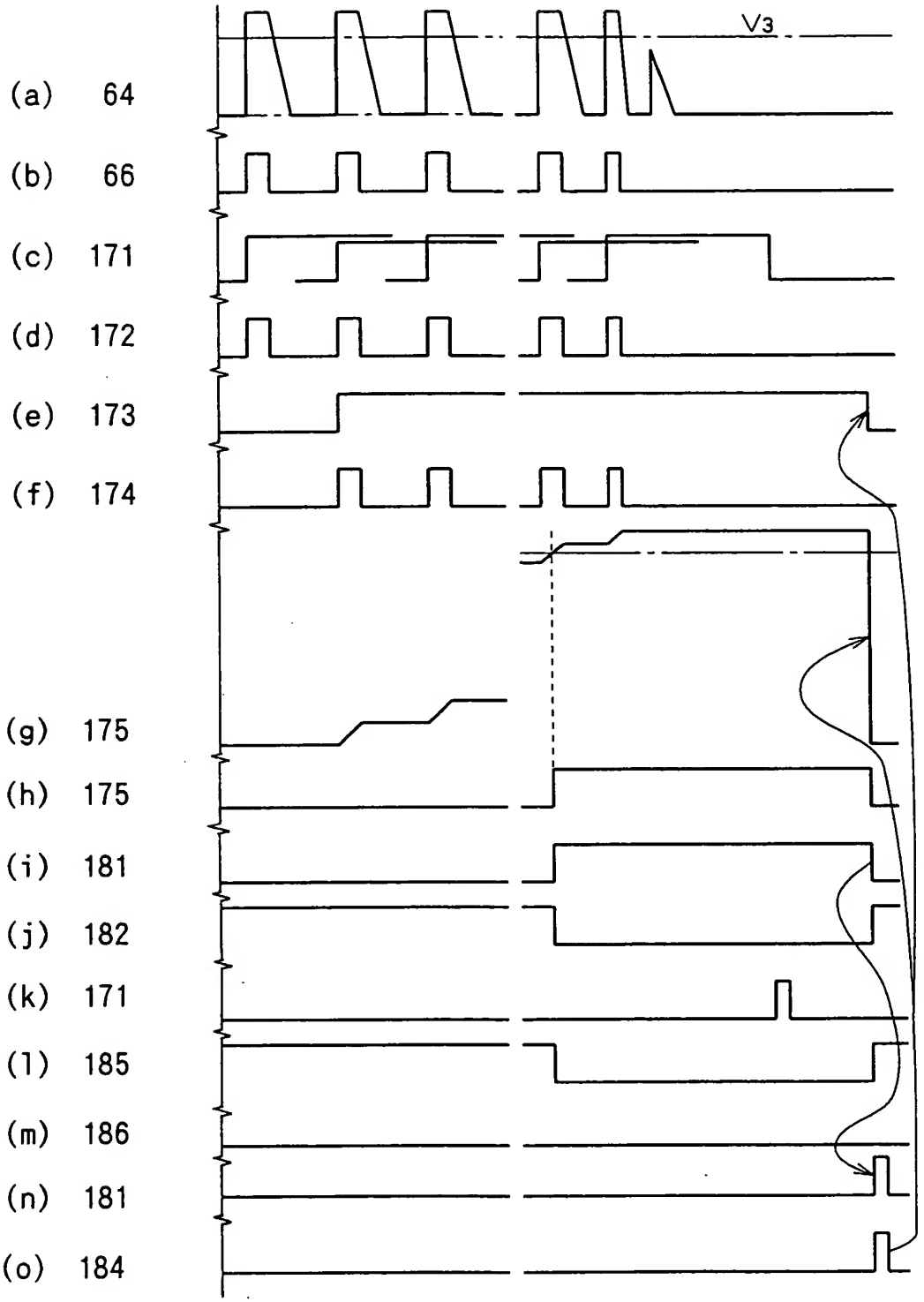

V3
(a) 64
(b) 66
(c) 171
(d) 172
(e) 173
(f) 174
(g) 175
(h) 175
(i) 181
(j) 182
(k) 171
(l) 185
(m) 186
(n) 181
(o) 184

FIG. 20

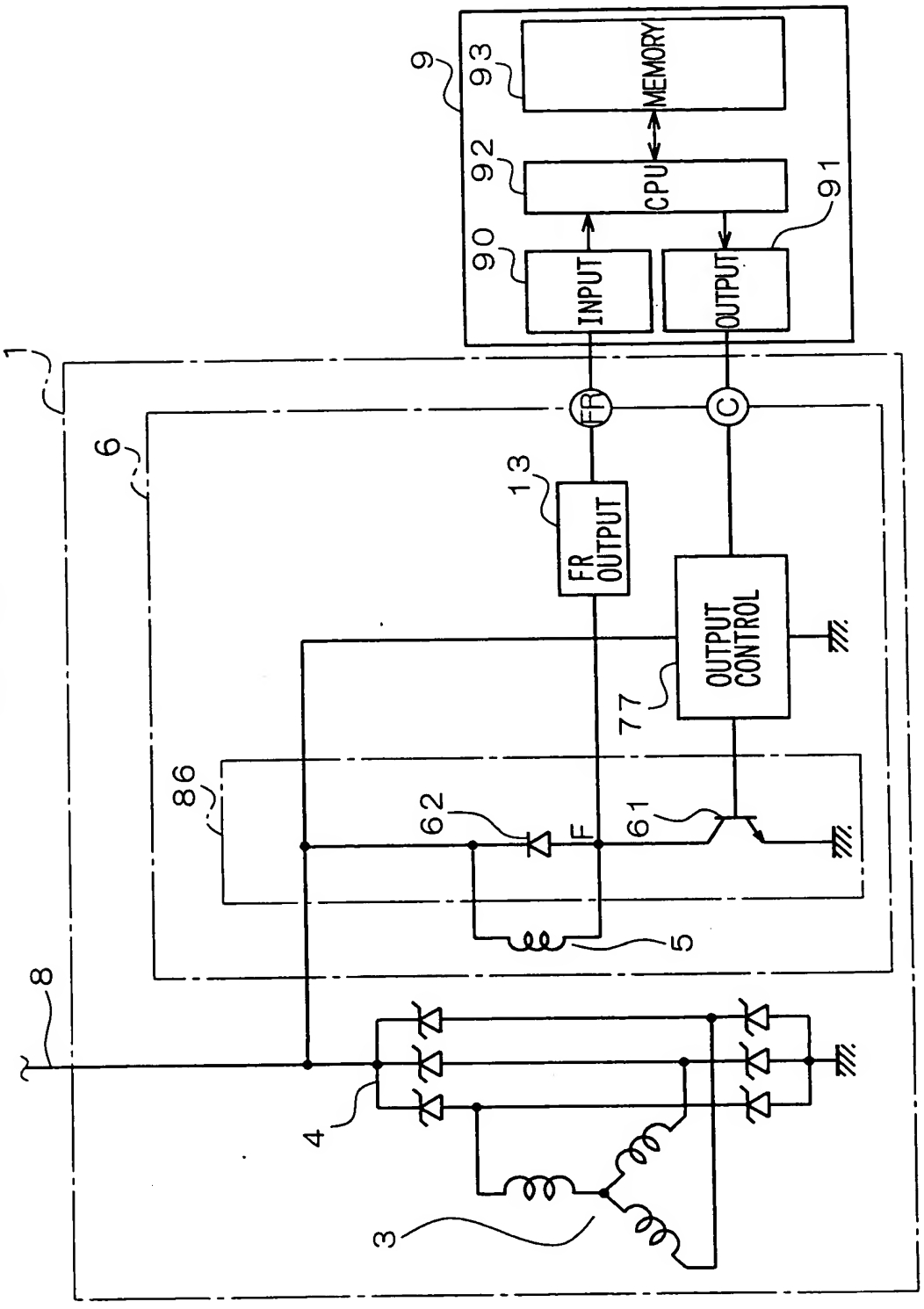
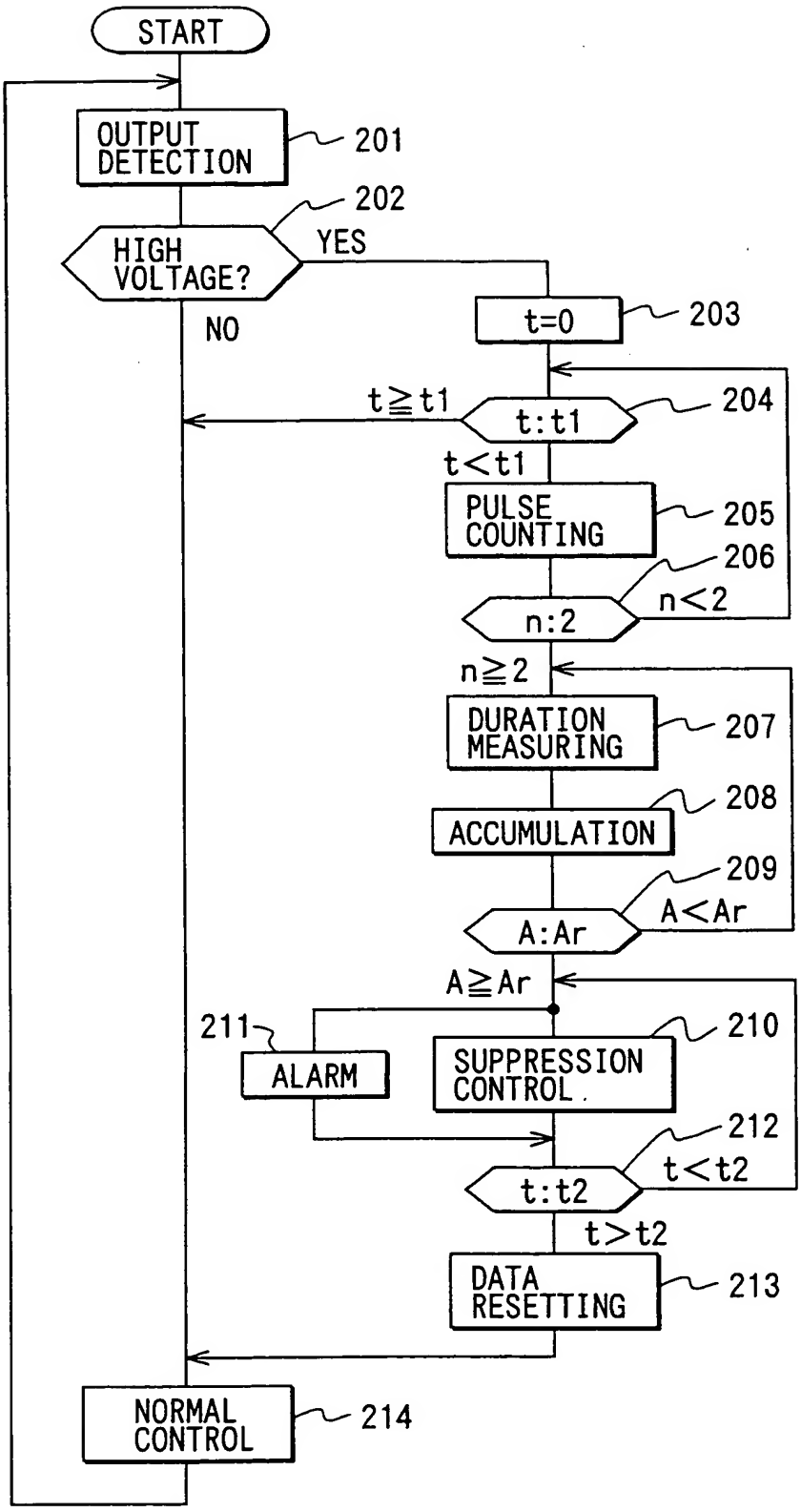

9
93
MEMORY
92
CPU
91
90
INPUT
OUTPUT
1
FR
C
6
13
FR OUTPUT
OUTPUT CONTROL
77
86
62
F
61
5
8
4
3

FIG. 21


START
OUTPUT DETECTION
201
202
HIGH VOLTAGE?
YES
NO
t=0
203
t≧t1
t:t1
204
t<t1
PULSE COUNTING
205
206
n:2
n<2
n≧2
DURATION MEASURING
207
ACCUMULATION
208
209
A:Ar
A<Ar
A≧Ar
211
ALARM
SUPPRESSION CONTROL
210
212
t:t2
t<t2
t>t2
DATA RESETTING
213
NORMAL CONTROL
214